	Type	Hits	Search Text	DBs	Time Stamp
1	IS&R	1226	(257/204,305,532).CCLS.	USPAT; US-PGPUB	2003/04/10 09:07
2	BRS	97	((257/204,305,532).CCLS.) and @pd>20021107	USPAT; US-PGPUB	2003/04/10 09:07
3	BRS	445	locos near5 thick$3	USPAT; US-PGPUB	2003/04/10 09:16
4	BRS	317	(locos near5 thick$3) and @pd<20010101	USPAT; US-PGPUB	2003/04/10 09:16
5	BRS	58	((locos near5 thick$3) and @pd<20010101) and dram	USPAT; US-PGPUB	2003/04/10 09:17

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
1	US 6545305 B1	12	Linear capacitor and process for making same	257/296	257/306; 257/532	Randazzo, Todd A.
2	US 5792680 A	36	Method of forming a low cost DRAM cell with self aligned twin tub CMOS devices and a pillar shaped capacitor	438/210	257/E21.645; 257/E21.648; 257/E27.089; 438/239; 438/255	Sung, Janmye et al.